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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/690,207	10/17/2000	Jean Francois Le Pennec	FR9-1999-0079 US1	2162

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EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/690,207	LE PENNEC ET AL.	
	Examiner	Art Unit	
	Robert W Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9,11-13 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9,11-13 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1.0 The application of Jean Francois Le Pennec et. al. entitled "METHOD AND SYSTEM FOR ESTABLISHING A VIRTUAL PATH CAPABILITY IN A FRAME RELAY NETWORK" filed on 10/17/2000 and amended on 7/6/04 which requests foreign priority based upon EPO 99480112.4 was examined. Claims 1-3, 5-9, 11-13, & 15-20 are pending.

Upon a further search the examiner discovered the prior art of Bosloy (U.S. Patent No.: 6,714,544 B1) and Bradley (U.S. Patent No.; 6,366,580 B1); consequently, the examiner withdraws the previous rejection and replaces it with this new rejection.

Claim Rejections - 35 USC § 103

2.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.0 **Claims 1-3, 5-9, 11-13, & 15-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherukuri et. al. (U.S. Patent No.: 6,125,119) in view of Bosloy et. al. (U.S. Patent No.: 6,714,544 B1).

Referring to **Claim 1**, Cherukuri teaches: A method for establishing a virtual path within a frame relay network wherein frames are transmitted over a plurality of virtual circuits from a first switching node to a second switching node (20 or first node transmits to 22 or second node per Fig 1)

Transmitting by said first switching node to said second switching node (20 or first node transmits to 22 or second node per Fig 1), a first control message transmitting a virtual path to be established (control message per col. 5 line 5 col. 6 line 44 or Table 3), and specifying two or more virtual circuits to be combined to form said virtual path to from said virtual path, said (SPVC or SVC between 20 and 22 per Fig 1) said information comprising:

Receiving a frame, at said second switching node (22 or second switching node receives a frame with SVPC or SVC per Fig 1 or Abstract or col. 1 line 15) wherein said frame has an identifier corresponding to said virtual path (It would have been obvious to one of ordinary skill in the art

at the time of the invention that an SVC or SVPC identifier would have had to been sent in order for the invention to work)

Forwarding said frame, utilizing said second switching node, to a destination determined based said two or more virtual circuits specified in said first control message 22 or 2nd node forwards the frame to 12 per Fig 1)

Cherukuri does not expressly call for: specifying two or more virtual circuits to be combined to form said virtual path or a frame has an identifier corresponding to said virtual path but teaches a SVC or SPVC per Fig 1 or , said information comprising:

A source virtual circuit identifier, which corresponds to an input adapter of said first switching node.

A source port identifier, which corresponds to an input port of said first switching node;

A destination virtual circuit identifier which corresponds to an output adapter of said second switching node; and

And a destination port identifier, which corresponds o an output port of said second switching node.

Bosloy teaches: specifying two or more virtual circuits to be combined to form said virtual path (col. 1 line 6-col. 7 line 35) and

A source virtual circuit identifier, which corresponds to an input adapter of said first switching node (The reference teaches that the ATM Forum defined a PNNI specification which defines set up messages associated with SVC processing. The specification recognizes that port, slot, VPI/VCI, destination address and destination address would be included in these messages and that these messages could also be utilized for frame relay upon replacing VPI/VCI with DLCI per col. 2 line 1 –col. 6 line 67. It would have been obvious to one of ordinary skill in the art at the time of the invention that a source address or source virtual circuit identifier would be present in order to determine the source node for the VPI/VCI which is replaced by the DLCI)

A source port identifier, which corresponds to an input port of said first switching node (The reference teaches that the PNNI ATM forum which is a standard has defined slots, ports, VCI, VPI, and port numbers could be inserted into the set up message per col. 5 line 1-col. 6 line 14 and that this same setup message could be utilized in Frame Relay where DLCI replaces VPI/VCI per col. 6 line 10-col. 7 line 17. It would have been obvious to one of ordinary skill in the art at the time of the invention that a source port identifier could be sent based upon the ATM forum teaching in order to speed up processing.)

A destination virtual circuit identifier which corresponds to an output adapter of said second switching node (The reference teaches that the ATM Forum defined a PNNI specification which

defines set up messages associated with SVC processing. The specification recognizes that port, slot, VPI/VCI, destination address and destination address would be included in these messages and that these messages could also be utilized for frame relay upon replacing VPI/VCI with DLCI per col. 2 line 1 –col. 6 line 67. It would have been obvious to one of ordinary skill in the art at the time of the invention that the destination address performs the same function as the destination virtual circuit identifier)

And a destination port identifier, which corresponds o an output port of said second switching node. (The reference teaches that the ATM Forum defined a PNNI specification which defines set up messages associated with SVC processing. The specification recognizes that port, slot, VPI/VCI, destination address and destination address would be included in these messages and that these messages could also be utilized for frame relay upon replacing VPI/VCI with DLCI per col. 2 line 1 –col. 6 line 67. It would have been obvious to one of ordinary skill in the art at the time of the invention that a destination port would perform the same function as a destination port identifier.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add specifying two or more virtual circuits as well as the ATM PNNI forum recommendations of Bosloy to be combined to form said virtual path and SVC identifier of Cherukuri in order to speed up processing.

Referring to **Claim 11**, Cherukuri teaches: A system of establishing a virtual path within a frame relay (Fig 1)

A frame relay network including a plurality of virtual circuits for transmitting frames from a first switching node to a second switching node (20 or first switching node transmitting frames to 22 or second switching node including SPVC or SVC or virtual circuit per Fig 1)
A virtual path established by a first control message transmitted by said first switching node to said second switching node (20 or first switching node establishes a virtual path to 22 or second switching node per Fig 1 utilizing a control message per col. 3 line 39-col. 6 line 44 or Table 3) and specifying two or more virtual circuits to be combined to form said virtual path (Fig 1)
A frame, having an identifier corresponding to said defined virtual path (It would have been obvious to one of ordinary skill in the art at the time of the invention that an SVC or SVPC identifier would have had to been sent in order for the invention to work), received by sadi second switching node and then forward said frame to a destination determined by said two or more virtual circuits specified in said control message (22 or 2nd node forwards the frame to 12 per Fig 1)

Cherukuri does not expressly call for: specifying two or more virtual circuits to be combined to form said virtual path or a frame has an identifier corresponding to said virtual path but teaches a SVC or SPVC per Fig 1

Cherukuri does not expressly call for: specifying two or more virtual circuits to be combined to form said virtual path or a frame has an identifier corresponding to said virtual path but teaches a SVC or SPVC per Fig 1, said information comprising:

A source virtual circuit identifier, which corresponds to an input adapter of said first switching node.

A source port identifier, which corresponds to an input port of said first switching node;

A destination virtual circuit identifier which corresponds to an output adapter of said second switching node; and

And a destination port identifier, which corresponds o an output port of said second switching node.

Bosloy teaches: specifying two or more virtual circuits to be combined to form said virtual path (col. 1 line 6-col. 7 line 35).

A source virtual circuit identifier, which corresponds to an input adapter of said first switching node (The reference teaches that the ATM Forum defined a PNNI specification which defines set up messages associated with SVC processing. The specification recognizes that port, slot, VPI/VCI, destination address and destination address would be included in these messages and that these messages could also be utilized for frame relay upon replacing VPI/VCI with DLCI per col. 2 line 1 –col. 6 line 67. It would have been obvious to one of ordinary skill in the art at the time of the invention that a source address or source virtual circuit identifier would be present in order to determine the source node on an input adapter of a switching node and for the VPI/VCI which is replaced by the DLCI)

A source port identifier, which corresponds to an input port of said first switching node (The reference teaches that the PNNI ATM forum which is a standard has defined slots, ports, VCI, VPI, and port numbers could be inserted into the set up message per col. 5 line 1-col. 6 line 14 and that this same setup message could be utilized in Frame Relay where DLCI replaces VPI/VCI per col. 6 line 10-col. 7 line 17. It would have been obvious to one of ordinary skill in the art at the time of the invention that a source port identifier could be sent based upon the ATM forum teaching in order to speed up processing.)

A destination virtual circuit identifier which corresponds to an output adapter of said second switching node (The reference teaches that the ATM Forum defined a PNNI specification which defines set up messages associated with SVC processing. The specification recognizes that port, slot, VPI/VCI, destination address and destination address would be included in these messages and that these messages could also be utilized for frame relay upon replacing VPI/VCI with DLCI per col. 2 line 1 –col. 6 line 67. It would have been obvious to one of ordinary skill in the art at the time of the invention that the destination address performs the same function as the destination virtual circuit identifier); and

And a destination port identifier, which corresponds o an output port of said second switching node. (The reference teaches that the ATM Forum defined a PNNI specification which defines set up messages associated with SVC processing. The specification recognizes that port, slot, VPI/VCI, destination address and destination address would be included in these messages and that these messages could also be utilized for frame relay upon replacing VPI/VCI with DLCI per col. 2 line 1 –col. 6 line 67. It would have been obvious to one of ordinary skill in the art at the time of the invention that a destination port would perform the same function as a destination port identifier.)

It would have been obvious to one of ordinary skill in the art at the time of the invention to add specifying two or more virtual circuits as well as the ATM PNNI forum recommendations of Bosloy to be combined to form said virtual path and SVC identifier of Cherukuri in order to speed up processing.

In Addition Dependent Claim limitations taught by Cherukuri:

Regarding **Claims 2 & 12**, wherein said control message includes a data link connection identifier corresponding to a predetermined value, for identifying said purpose of first control message (col. 1 line 15-col. 2 line 10)

Regarding **Claims 5 & 15**, further comprising the step of: transmitting by said second switching node to said first switching node (22 or second switching node to 20 of first switching node per Fig 1), a second control message conveying acknowledgement of said request to establish said virtual path (Activate received or acknowledgement per Table 3 or col. 3 line 39-col. 6 line 44) or rejection of said request to establish said virtual path (Deactivate received or rejection per Table 3 or col. 3 line 39-col. 6 line 44)

Regarding **Claims 6 & 16**, transmitting to said first switching node to said second switching node (transmitting from 20 of first switching node to 22 or second switching node per Fig 1), a third control message acknowledging a reception of said second control message by said first switching node (Activate received or acknowledgment or third control message per Table 3 or col. 3 line 39-col. 6 line 44)

Regarding **Claims 7 & 17**, further comprising the step of: starting a timeout timer, by said first switching node, when said first control message is transmitted (Figs 4-8)

Detecting an error when said timeout timer expires prior to receiving a second control message from said second switching node, wherein said second control message conveys acknowledgement of said request to establish said virtual path or rejection of said request to establish said virtual path (Figs 4-8)

Regarding **Claims 8 & 18**, transmitting to said second switching node, a forth control message, sent by said first switching network, for removing one of said two or more virtual circuits from said virtual path (deactivate pending or deactivate receiver or control message for canceling said virtual path per Table 3 or Abstract)

Regarding **Claims 9 & 19**, further comprising the step of :

Transmitting to said second switching (22 per Fig 1 or second switch) a fifth control message, sent by said first switching network , for canceling said virtual path (deactivate pending or deactivate receiver or control message for canceling said virtual path per Table 3 or Abstract)

In Addition Bosloy teaches:

Regarding **Claims 3 & 13**, wherein said step of transmitting said first control message includes the step of transmitting a field for identifying each of said two or more said virtual circuits. (The reference teaches DLCI or identifier two or more virtual circuits per col. 1 line 6-col. 7 line 35.)

Claim Rejections - 35 USC § 103

4.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.0 **Claims 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Cherukuri et. al. (U.S. Patent No.; 6,125,119) in view of Bosloy et. al. (U.S. Patent No.: 6,714,544 B1) further in view of Bradley (U.S. Patent No.; 6,366,580 B1).

Referring to **Claim 20,** the combination of Cherukuri and Bosloy teach: the system of Claim 18, further comprising:

The combination of Cherukuri and Bosloy do not expressly call for: a plurality of activities timers, wherein one said activities timers corresponds to each of said two or more virtual circuits combined to form said virtual path, wherein for each frame received for said two or more virtual circuits combined to form said virtual path, said corresponding said activity-timer is reset;

An error condition signal, wherein said error condition signal is generated from the detection by the expiration of one of said activity-timers, an extended period of non-activity by one of said virtual circuits which correspond to said expired activity-timer, and

A fourth control message, sent by said first switching network in response to said error condition signal, for removing from said virtual path, said virtual circuit corresponding to said expired activity-timer but Bosloy teaches that ATM messaging concepts can be applied to Frame Relay

Bradley teaches: a plurality of activities timers, wherein one said activities timers corresponds to each of said two or more virtual circuits combined to form said virtual path, wherein for each frame received for said two or more virtual circuits combined to form said virtual path, said corresponding said activity-timer is reset (Activities timers per Figures 1-3 or per col. 4 line 13-col. 5 line 6);

An error condition signal, wherein said error condition signal is generated from the detection by the expiration of one of said activity-timers, an extended period of non-activity by one of said virtual circuits which correspond to said expired activity-timer (timer expires on associated with an SVC before and ACK received results in a SVC being terminated per Figures 1-3 or per col. 4 line 13-col. 5 line 6); and

A fourth control message, sent by said first switching network in response to said error condition signal, for removing from said virtual path, said virtual circuit corresponding to said expired activity-timer (timer expires on associated with an SVC before and ACK received results in a SVC being terminated or a message to tear the SVC down per Figures 1-3 or per col. 4 line 13-col. 5 line 6);

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the activities timer, error condition, and control messaging of Bradley to the system of the combination of Cherukuri and Bosloy which sets up and processes SVC because Bosloy taught that ATM setup messaging concepts can be applied to Frame Relay.

Conclusion

6.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on 571/272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2661

RWW
October 28, 2004

KENNETH VANDERPUYE
PRIMARY EXAMINER